

Title (en)

ARRANGEMENT FOR PACKING HIGH-SPEED INTEGRATED CIRCUITS, INCLUDING DECOUPLING CAPACITORS FOR THE POWER INPUT TERMINALS, AND METHOD FOR REALIZING IT.

Publication

EP 0000384 B1 19811230 (DE)

Application

EP 78100332 A 19780707

Priority

US 81595177 A 19770715

Abstract (en)

[origin: US4153988A] A high performance package for integrated circuit semiconductor devices in which decoupling capacitors are provided in close proximity to the integrated circuit devices for reducing voltage variations in the power driver lines, and/or a ground plate overlying the stripe metallurgy on the surface of the substrate for reducing cross-talk between signal lines. The decoupling capacitors are each comprised of a conductive layer on the inside of a via hole, a concentric dielectric layer on the conductive layer, and an electrically conductive plug in physical contact with the dielectric layer that is associated with the driver line circuitry of the package.

IPC 1-7

H01L 23/56

IPC 8 full level

H01L 23/02 (2006.01); **H05K 1/16** (2006.01); **H01L 23/12** (2006.01); **H01L 23/52** (2006.01); **H01L 23/64** (2006.01); **H01L 25/00** (2006.01); **H05K 1/18** (2006.01)

CPC (source: EP US)

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C-Set (source: EP US)

H01L 2924/0002 + H01L 2924/00

Cited by

EP0083405A3; EP1001464A1; EP0573838A3; EP0483946A1; DE102014004660A1; US6469331B2; DE102014008858A1

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EP 78100332 A 19780707; CA 305588 A 19780615; DE 2861463 T 19780707; IT 2489378 A 19780623; JP 7660878 A 19780626; US 81595177 A 19770715