

Title (en)  
**A COMPOSITE JFET-BIPOLAR STRUCTURE**

Publication  
**EP 0000975 B1 19820106 (EN)**

Application  
**EP 78200164 A 19780829**

Priority  
US 82899977 A 19770830

Abstract (en)  
[origin: US4143392A] A junction field effect transistor and a bipolar transistor are merged in a single composite device disposed within a single isolation region by the use of planar processing techniques. The device includes an annular source region (20) formed within a semiconductor body portion (12) constituting a collector zone. Within the central portion of the collector zone circumscribed by the annular source region there is formed an emitter zone (24) nested within a region (22) that constitutes both the drain region of the JFET and the base zone of the bipolar transistor. An annular channel region (28) connects the annular source region (20) and the central drain region (22). An annular region (30) forming a semiconductor junction with the annular channel (28) adjacent to the annular source region (20) constitutes one of two gate regions of the JFET. The other gate region is constituted by the body portion (12) serving as the collector zone.

IPC 1-7  
**H01L 27/06**

IPC 8 full level  
**H01L 21/331** (2006.01); **H01L 21/337** (2006.01); **H01L 21/8222** (2006.01); **H01L 21/8248** (2006.01); **H01L 27/06** (2006.01); **H01L 27/07** (2006.01); **H01L 29/73** (2006.01); **H01L 29/80** (2006.01); **H01L 29/808** (2006.01)

CPC (source: EP US)  
**H01L 27/0716** (2013.01 - EP US)

Cited by  
EP0435541A3; EP0064870B1

Designated contracting state (EPC)  
DE FR GB

DOCDB simple family (publication)  
**EP 0000975 A1 19790307**; **EP 0000975 B1 19820106**; DE 2861510 D1 19820225; JP S5452994 A 19790425; JP S6153861 B2 19861119; US 4143392 A 19790306

DOCDB simple family (application)  
**EP 78200164 A 19780829**; DE 2861510 T 19780829; JP 10618678 A 19780830; US 82899977 A 19770830