

Title (en)  
Substrate bias regulator.

Title (de)  
Substrat-Vorspannungsregler.

Title (fr)  
Régulateur de polarisation de substrat.

Publication  
**EP 0015342 A1 19800917 (EN)**

Application  
**EP 79302875 A 19791212**

Priority  
US 1752379 A 19790305

Abstract (en)  
A substrate bias regulator 11 useful for controlling a variable output oscillator 12 and/or a substrate bias voltage generator 13 is provided to control the substrate voltage on a semiconductor chip 10. A series of field effect transistors are arranged in a manner to sense the substrate voltage and to provide an output to regulate the substrate voltage. One of the series field effect transistors 16, 32 has its gate electrode connected to reference potential ground which tends to make the regulator independent of transistor thresholds.

IPC 1-7  
**G05F 3/20**

IPC 8 full level  
**G11C 11/407** (2006.01); **G05F 3/20** (2006.01); **H01L 21/822** (2006.01); **H01L 27/04** (2006.01); **H01L 29/78** (2006.01)

CPC (source: EP)  
**G05F 3/205** (2013.01)

Citation (search report)  

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- FR 2235417 A1 19750124 - IBM [US]
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- IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE, Digest on Technical Papers, Vol. 19, February 18, 1976 New York US E. BLASER: "Substrate and Load Gate Voltage Compensation", pages 56 and 57. \* The whole article \*
- IBM TECHNICAL DISCLOSURE BULLETIN, Vol. 19, December 1976 New York US E. BLASER: "Substrate Compensation for Depletion-Mode FET Circuits", page 2530 and page 2531 \* The whole article \*

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Designated contracting state (EPC)  
DE FR GB

DOCDB simple family (publication)  
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DOCDB simple family (application)  
**EP 79302875 A 19791212**; DE 2966592 T 19791212; JP 2518580 A 19800229