Title (en)

TWO-MODE-SHIFT REGISTER/COUNTER DEVICE

Publication

EP 0017091 B1 19830608 (EN)

Application

EP 80101464 A 19800320

Priority

US 2814679 A 19790409

Abstract (en)

[origin: EP0017091A1] Data processing apparatus constructed in shift register logic is provided in a simple manner with an optional pulse counting function by incorporating additional switching logic (64) into a linear shift register of sequential stages (SRL 0, 1, 2, 3) thereof, the additional logic (64) being responsive to a pulse input (C CLOCK), a count enable input and the current stage of the stages to force Grey code pattern shifting within separate groups (COUNTER SEG 1, 2) of sequentially adjacent stages and pulse advance between each sequentially adjacent pair of the groups at the termination of each Grey code pattern cycle in the leading group of the pair. Both the linear shift function and the counting function are provided with the worst case inter stage connection spanning no more than a group.

IPC 1-7

G06F 7/00; G11C 19/00

IPC 8 full level

G01R 31/3185 (2006.01); **G11C 19/00** (2006.01); **H03K 23/00** (2006.01); **H03K 23/54** (2006.01); **H03K 23/58** (2006.01)

CPC (source: EP US)

G01R 31/318527 (2013.01 - EP US); **G11C 19/00** (2013.01 - EP US); **H03K 23/005** (2013.01 - EP US); **H03K 23/54** (2013.01 - EP US); **H03K 23/542** (2013.01 - EP US)

Cited by

EP0064590A1; EP0358365A3; EP0057314A1

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EP 0017091 A1 19801015; **EP 0017091 B1 19830608**; DE 3063649 D1 19830714; JP S55135424 A 19801022; JP S6156903 B2 19861204; US 4264807 A 19810428

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