

Title (en)

MONOLITHIC INTEGRATED SEMICONDUCTOR CIRCUIT WITH CLOCK PULSE CONTROLLED SHIFT REGISTER

Publication

**EP 0017245 A3 19811202 (DE)**

Application

**EP 80101822 A 19800403**

Priority

DE 2914518 A 19790410

Abstract (en)

[origin: US4403334A] A monolithically integrable semiconductor circuit having an input section into which respective electrical signals which are to be evaluated and which have been provided by groups of binary pulses are serially feedable, includes a clock-controlled shift register in the input section, the shift register being operable by shift pulses from the controlling clock thereof. The shift register has a plurality of register cells corresponding in number at least to the number of binary digits of the groups of binary pulses. The semiconductor circuit also includes a logic circuit, at least two of the register cells having an output operatively connected to the logic circuit for controlling the logic circuit. A pulse counter is driven by the shift pulses as counting pulses, the logic circuit having an output operatively connected to the pulse counter for fixing the count thereof, and at least one other circuit component is controllable by the count of the pulse counter respectively fixed by the control of the logic circuit.

IPC 1-7

**G10H 1/36; G11C 19/28**

IPC 8 full level

**G10H 1/36** (2006.01)

CPC (source: EP US)

**G10H 1/36** (2013.01 - EP US)

Citation (search report)

- US 3889568 A 19750617 - AMAYA TOSHIYUKI
- US 4142433 A 19790306 - GROSS ULRICH
- US 3530284 A 19700922 - WOOD DELLOS L
- IBM TECHNICAL DISCLOSURE BULLETIN, Band 19. No. 7, Dezember 1976 New York (US) E.C. DUNN et al.: "Ring counter checking circuits", Seiten 2460-2461 \* Seite 2461, Zeilen 11-13 \*

Designated contracting state (EPC)

FR GB

DOCDB simple family (publication)

**EP 0017245 A2 19801015; EP 0017245 A3 19811202; EP 0017245 B1 19850731; DE 2914518 A1 19801023; JP S55140900 A 19801104; US 4403334 A 19830906**

DOCDB simple family (application)

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