

Title (en)  
Processor on a single semiconductor substrate.

Title (de)  
Rechner auf einem einzigen Halbleitersubstrat.

Title (fr)  
Processeur sur un seul substrat semiconducteur.

Publication  
**EP 0031889 A1 19810715 (EN)**

Application  
**EP 80107147 A 19801118**

Priority  
US 10571179 A 19791220

Abstract (en)  
[origin: ES8106810A1] A processor is provided that is fabricated on a single semiconductor substrate. The processor includes an AND array for receiving program instructions from input sources external of the processor and for generating product signals. An OR array is provided and interconnected to the AND array for receiving the product signals and for generating a plurality of control signals. A register array receives ones of the plurality of control signals and transfers data between the processor and data sources external of the processor. An arithmetic and logic unit array is also provided on the semiconductor substrate and interconnected to the register array and the OR array for executing operations on data received from the register array in accordance with ones of the plurality of control signals to generate output data. A control register is further provided and is interconnected to the OR array and the AND array for receiving ones of the plurality of control signals for controlling execution of the program instructions within the AND array.

IPC 1-7  
**G06F 9/22**

IPC 8 full level  
**G06F 7/00** (2006.01); **G06F 9/22** (2006.01); **G06F 15/78** (2006.01)

CPC (source: EP US)  
**G06F 9/223** (2013.01 - EP US)

Citation (search report)

- US 3983538 A 19760928 - JONES JOHN W
- IBM TECHNICAL DISCLOSURE BULLETIN, Vol. 22, No. 6, November 1979, New York, USA MANNING et al. "Microprogrammed processor having PLA control store", page 2440-2441. \* Complete article \*
- IEEE JOURNAL OF SOLID STATE CIRCUITS, Vol. 14, No. 5, October 1979, New York, USA COOK et al: "A study in the use of PLA-based macros", pages 833-840. \* Page 833, right-hand column, last paragraph - page 834, left-hand column, 1st paragraph; page 838, left-hand column, 2nd paragraph - page 839, left-hand column, 1st paragraph \*
- IEEE JOURNAL OF SOLID STATE CIRCUITS, Vol. SC-10, No. 5, October 1975 New York, USA HORNINGER: "A high-speed EFSI SOS programmable logic array with an MNOS version", pages 331-336. \* Page 332, right-hand column, 2nd paragraph - page 333, left-hand column, 1st paragraph \*
- ELECTRONICS, Vol. 43, No. 7, March 30, 1970, New York, USA "MOS array is custom programmable" pages 133-134. \* Page 133, righthand column, 1st paragraph \*
- IBM TECHNICAL DISCLOSURE BULLETIN, Vol. 21, No. 4, September 1978, New York, US DANSKY et al. "Custom programmable logic arrays on STL masterslices", pages 1456-1460. \* Page 1459, 2nd paragraph \*

Cited by  
EP0087005A3; EP0199173A3; EP0082328A1; DE3138971A1; EP0071727A1; EP0075623A1; WO8301325A1; EP0075624B1

Designated contracting state (EPC)  
BE CH DE FR GB IT NL SE

DOCDB simple family (publication)  
**EP 0031889 A1 19810715; EP 0031889 B1 19841024;** AU 534788 B2 19840216; AU 6321280 A 19810625; BR 8008307 A 19810707; CA 1149071 A 19830628; DE 3069518 D1 19841129; ES 497082 A0 19810801; ES 8106810 A1 19810801; JP S5690342 A 19810722; JP S6211733 B2 19870314; US 4354228 A 19821012

DOCDB simple family (application)  
**EP 80107147 A 19801118;** AU 6321280 A 19801013; BR 8008307 A 19801218; CA 363530 A 19801029; DE 3069518 T 19801118; ES 497082 A 19801124; JP 12808480 A 19800917; US 10571179 A 19791220