Title (en)

INTEGRATED MOS SEMICONDUCTOR CIRCUIT

Publication

EP 0036494 B1 19840725 (DE)

Application

EP 81101324 A 19810224

Priority

DE 3009303 A 19800311

Abstract (en)

[origin: US4454431A] A semiconductor circuit assembly having capacitively controlled field effect transistors, includes a semiconductor chip containing a digital circuit part for supplying timing pulses for controlling operation of the digital circuit part, and terminal having at least one conductive connection to the digital circuit part and the timing pulse generator for supplying potentials thereto from a direct current source. An oscillator is provided and a substrate-bias generator connected to the oscillator and the timing pulse generator. The substrate-bias generator is controlled by the oscillator for producing a bias voltage able to reach a given full value and for activating the timing pulse generator only after the substrate bias voltage has reached its full value.

IPC 1-7

G05F 3/20

IPC 8 full level

G11C 11/407 (2006.01); **G05F 3/20** (2006.01); **G11C 11/34** (2006.01); **H01L 21/822** (2006.01); **H01L 27/04** (2006.01); **H01L 27/10** (2006.01)

CPC (source: EP US)

G05F 3/205 (2013.01 - EP US)

Cited by

EP0175152A3; EP0217065A1

Designated contracting state (EPC)

DE FR GB IT

DOCDB simple family (publication)

EP 0036494 A2 19810930; **EP 0036494 A3 19811125**; **EP 0036494 B1 19840725**; DE 3009303 A1 19810924; DE 3164950 D1 19840830; JP H0213821 B2 19900405; JP S56142663 A 19811107; US 4454431 A 19840612

DOCDB simple family (application)

EP 81101324 A 19810224; DE 3009303 A 19800311; DE 3164950 T 19810224; JP 3372081 A 19810309; US 24019781 A 19810303