

Title (en)

Read only storage matrix.

Title (de)

Festwertspeichermatrix.

Title (fr)

Matrice de mémoire morte.

Publication

EP 0041603 A1 19811216 (EN)

Application

EP 81102886 A 19810415

Priority

US 15792180 A 19800609

Abstract (en)

[origin: US4347585A] This matrix has high barrier Schottky diodes at Read or Reproduce Only Storage (ROS) matrix crossovers to represent 1's (the absence of diodes representing 0's) and low barrier Schottky diodes connected to select individual column lines (bit lines) of the ROS matrix. A current sink is connected to each column. Any unselected column causes the current in that column to be diverted through the respective low barrier diode, thus preventing that current from flowing into the selected word line. The only current that flows into the selected word line of a matrix depends from the single selected column current source.

IPC 1-7

G11C 17/06

IPC 8 full level

G11C 17/06 (2006.01); **G11C 17/08** (2006.01)

CPC (source: EP US)

G11C 17/06 (2013.01 - EP US); **G11C 17/08** (2013.01 - EP US)

Citation (search report)

- US 4196363 A 19800401 - MALAVIYA SHASHI D [US]
- FR 2313820 A1 19761231 - SIEMENS AG [DE]
- US 4070654 A 19780124 - TACHI SEIICHI
- US 3924264 A 19751202 - DORLER JACK A, et al
- US 3780320 A 19731218 - DORLER J, et al
- US 4099260 A 19780704 - LYNES DENNIS JOSEPH, et al
- Computer Vol. 10, No. 7, July 1977, New York (US) J.F. GUNN et al.: "A Bipolar 16K Rom Utilizing Schottky Diode Cells" pages 14-17 * page 16, paragraph "Access Circuits, the Key to High Performance"; figure 4 * & US - A - 4 099 260 (Bell)
- IBM Technical Disclosure Bulletin Vol. 21, No. 10, March 1979 Armonk (US) F. Montegari et al.: "Array Precharge Circuit" pages 4057-4058 * figures 1-2 *
- IBM Technical Disclosure Bulletin Vol. 22, No. 12, May 1980 Armonk (US) F.A. MONTEGARI et al.: "Schottky Barrier Diode Read-Only Store" pages 5369-5370 * page 5369, lines 1-7; figure 1 *
- IBM Technical Disclosure Bulletin Vol.20, No.8, January 1978, Armonk (US) J. PERRIS et al.: "Precharge Circuit for Memory Array Bit Lines" pages 3138-3139 *the whole article*
- IBM Technical Disclosure Bulletin Vol. 20, No. 11A, April 1978 Armonk (US) J. PERRIS et al.: "Bit Line Constant Current Source Switch for a Read-Only Store" pages 4412-4414 * the whole article *
- IEEE Journal of Solid-State Circuits, Vol.SC-15, No. 5, October 1980, New York (US) J.A. LUDWIG: "A 50K Bit Schottky Cell Bipolar Read-Only Memory" pages 816-820 *pages 816-817, paragraph "Memory Organization"; figures 1-2,4 and 6,*
- IEEE International Solid-State Circuits Conference, 14 February 1975, Digest of Technical Papers New York (US) A.W. PELTIER: "A New Approach to Bipolar LSI:C3L" pages 168-169
- IEEE International Solid-State Circuits Conference, 14 February 1975, Digest of Technical Papers New York (US) H.H. BERGER et al.: "Schottky Transistor Logic" pages 172-173
- IBM Technical Disclosure Bulletin Vol.17, No.10, March 1975 Armonk (US) V.L. GANI et al.: "Logic Circuit with Dual-Metal Schottky Barrier Diodes" page 2856
- IEEE Journal of Solid-State Circuits, Vol.SC-4, No.5, October 1969 New York (US) D.A. HODGES et al.: "Low-Power Bipolar Transistor Memory Cells" pages 280-284 *figure 3*

Cited by

EP0184138A3; US4935050A

Designated contracting state (EPC)

DE FR GB

DOCDB simple family (publication)

EP 0041603 A1 19811216; EP 0041603 B1 19840711; DE 3164678 D1 19840816; JP S578993 A 19820118; JP S5855599 B2 19831210;
US 4347585 A 19820831

DOCDB simple family (application)

EP 81102886 A 19810415; DE 3164678 T 19810415; JP 5067381 A 19810406; US 15792180 A 19800609