

Title (en)
SEMICONDUCTOR MEMORY DEVICE

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Application
EP 81305347 A 19811111

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Abstract (en)
[origin: EP0053878A2] A semiconductor memory device is constituted by a MOS transistor having a floating gate (FG) for storing data. An erase gate (EG) is arranged on the MOS transistor to discharge electrons from the floating gate. The MOS transistors are arranged in a matrix form in which the erase gates of all the MOS transistors are commonly connected and a data erase voltage is applied to the erase gates to erase the data.

IPC 1-7
G11C 11/34; H01L 29/60; H01L 27/10

IPC 8 full level
G11C 16/04 (2006.01); **G11C 16/16** (2006.01); **H01L 29/788** (2006.01)

CPC (source: EP US)
G11C 16/0416 (2013.01 - EP US); **G11C 16/16** (2013.01 - EP US); **H01L 29/7885** (2013.01 - EP US)

Citation (search report)
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• [XE] US 4357685 A 19821102 - DANIELE VINCENZO, et al
• [XE] EP 0047153 A1 19820310 - FUJITSU LTD [JP]
• [XP] INTERNATIONAL ELECTRON DEVICES MEETING, 8th-10th December 1980, pages 602-606, Washington D.C. (USA); J. KUPEC et al.: "Triple level poly silicon E2prom with single transistor per bit".
• [A] IEEE TRANSACTIONS ON ELECTRON DEVICES, vol. ED-27, no. 7, July 1980, pages 1211-1216, New York (USA); B. GERBER et al.: "Low-voltage single supply CMOS electrically erasable read-only memory".

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