

Title (en)  
DYNAMIC RANDOM ACCESS MEMORY.

Title (de)  
DYNAMISCHER SCHREIB-LESE-SPEICHER.

Title (fr)  
MEMOIRE A ACCES SELECTIF DYNAMIQUE.

Publication  
**EP 0054022 A4 19841105 (EN)**

Application  
**EP 80901815 A 19800602**

Priority  
US 8000673 W 19800602

Abstract (en)  
[origin: WO8103568A1] A dynamic random access memory (10) receives a memory address of a row decoder (14) which charges a selected row line (18). When the row line (18) is charged an access transistor (24) in a memory cell (22) is rendered conductive to connect a storage capacitor (26) to a bit line (30). The bit lines (30, 38) are previously set at an equilibration voltage. The voltage on the bit line (30) is driven slightly above the equilibration voltage if a high voltage state had been stored in the capacitor (26) or the voltage on the bit line is driven slightly below the equilibration voltage if a low voltage state had been stored on the capacitor (26). A sense amplifier (44) is connected to the bit lines (30, 38) and upon receipt of a latch signal (L) drives the one of the bit lines (30, 38) having the lower voltage to a low voltage state. A pullup circuit (60) drives the voltage on the remaining bit line of the pair to a high voltage state, restoring the memory storage capacitor (26) to its initial state. After the row line (18) is now discharged trapping the original data state in the storage capacitor (26), precharge transistors (50, 52) then connect together the bit lines (30, 38) through a latch node (46) to share charge between the bit lines (30, 38) and drive the bit lines (30, 38) to the equilibration voltage.

IPC 1-7  
**G11C 7/00**

IPC 8 full level  
**G11C 7/00** (2006.01); **G11C 11/34** (2006.01); **G11C 11/409** (2006.01); **G11C 11/4094** (2006.01)

CPC (source: EP)  
**G11C 11/4094** (2013.01)

Citation (search report)

- [Y] US 4107556 A 19780815 - STEWART ROGER GREEN, et al
- [Y] US 4004284 A 19770118 - HEEREN RICHARD H

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