

Title (en)
A SEMICONDUCTOR MEMORY DEVICE

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Application
EP 81305984 A 19811221

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Abstract (en)
[origin: US4476547A] The present invention discloses a memory cell layout of a dynamic RAM of a folded bit line type MOS FET wherein the bit line pairs are extended in parallel away from the sense amplifiers. The present invention includes a particular bit line pair and at least one bit line of an adjacent bit line pairs positioned between the particular bit line pair and makes the capacitor regions corresponding to the mutually adjacent bit lines interleave and thereby improves the area efficiency of the capacitor region.

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IPC 8 full level
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CPC (source: EP US)
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Cited by
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