Title (en)

A SEMICONDUCTOR MEMORY DEVICE

Publication

EP 0055572 B1 19860813 (EN)

Application

EP 81305984 A 19811221

Priority

JP 18893480 A 19801226

Abstract (en)

[origin: US4476547A] The present invention discloses a memory cell layout of a dynamic RAM of a folded bit line type MOS FET wherein the bit line pairs are extended in parallel away from the sense amplifiers. The present invention includes a particular bit line pair and at least one bit line of an adjacent bit line pairs positioned between the particular bit line pair and makes the capacitor regions corresponding to the mutually adjacent bit lines interleave and thereby improves the area efficiency of the capacitor region.

IPC 1-7

G11C 5/02

IPC 8 full level

G11C 7/18 (2006.01); **G11C 11/401** (2006.01); **G11C 11/4097** (2006.01); **H01L 21/822** (2006.01); **H01L 21/8242** (2006.01); **H01L 27/04** (2006.01); **H01L 27/10** (2006.01); **H01L 27/108** (2006.01)

CPC (source: EP US)

G11C 7/18 (2013.01 - EP US); **G11C 11/4097** (2013.01 - EP US)

Cited by

EP0293578A3; GB2220099A; GB2220099B; EP0420185A3; US5420816A; EP0399531A1; US5194752A; US5324975A; EP0264929A3

Designated contracting state (EPC)

DE FR GB

DOCDB simple family (publication)

US 4476547 A 19841009; DE 3175136 D1 19860918; EP 0055572 A2 19820707; EP 0055572 A3 19840411; EP 0055572 B1 19860813; IE 53051 B1 19880525; IE 813064 L 19820626; JP H0319710 B2 19910315; JP S57111061 A 19820710

DOCDB simple family (application)

US 32769181 A 19811204; DE 3175136 T 19811221; EP 81305984 A 19811221; IE 306481 A 19811223; JP 18893480 A 19801226