

Title (en)
DECODER CIRCUIT FOR SEMICONDUCTOR MEMORY.

Title (de)
DEKODIERUNGSKREIS FÜR HALBLEITERSPEICHER.

Title (fr)
CIRCUIT DECODEUR POUR MEMOIRE A SEMI-CONDUCTEUR.

Publication
EP 0056366 A4 19840913 (EN)

Application
EP 80901908 A 19800602

Priority
US 8000670 W 19800602

Abstract (en)
[origin: WO8103573A1] A decoder circuit (66) includes a plurality of input transistors (78-86) connected to address lines (68-76). The drain terminals of the input transistors (78-86) are connected to a first power terminal and the source terminals thereof are connected to a first node (92) which is charged to low voltage state upon receipt of a precharge signal at a transistor (94). An address enable signal (58) operates a transistor (96) to connect node (92) to node (98) during receipt of the address. A node (102) is charged to a high state by operation of a transistor (100) in response to a precharge signal (56). Node (102) is discharged through a transistor (104) when a high voltage state is present at the node (98). An enable clock signal (52) is transmitted through a transistor (106) to a row line (108) when a high voltage state is present on node (102).

IPC 1-7
G11C 11/40

IPC 8 full level
G11C 11/34 (2006.01); **G11C 8/00** (2006.01); **G11C 8/10** (2006.01); **G11C 11/418** (2006.01)

CPC (source: EP)
G11C 8/10 (2013.01); **G11C 11/418** (2013.01)

Citation (search report)
• [Y] US 4200917 A 19800429 - MOENCH JERRY D [US]
• [X] US 3702926 A 19721114 - PICCIANO JAMES K, et al
• [A] US 4074237 A 19780214 - SPAMPINATO DOMINIC PATRICK
• [X] PATENTS ABSTRACTS OF JAPAN, vol. 2, no. 84, page 3583 E 78; & JP - A - 53 48 423 (HITACHI SEISAKUSHO K.K.) 01-05-1978

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