Title (en)

CIRCUIT FOR DELAY NORMALISATION OF INTERCONNECTED SEMICONDUCTOR CIRCUITS

Publication

EP 0057351 B1 19840704 (DE)

Application

EP 82100160 A 19820112

Priority

US 22941781 A 19810129

Abstract (en)

[origin: US4383216A] An on chip delay regulator circuit which varies the power in logic or array circuits on the chip so as to minimize, or eliminate, chip to chip circuit speed differences caused by power supply variations and/or lot to lot process differences, temperature, etc. The on chip delay regulator accomplishes this by comparing a periodic reference signal to a periodic on chip generated signal which is sensitive to power supply changes, lot to lot process changes, temperature, etc. The comparison creates an error signal which is used to change the power (current or voltage) supplied to the on chip circuits. By changing the circuit power, the circuit speed (gate delay) is increased or decreased as necessary to maintain a relatively constant circuit speed on each chip. For example, a plurality of integrated circuit chips each contain an on chip delay regulator. The on chip delay regulator on each chip of said plurality of integrated circuit chips receives and responds to the same signal (or clock). Each chip provides a discrete on chip generated signal related to the parameters of the chip. The gate delay (or speed) of the circuitry on each chip is determined by its on chip delay regulator under control of the common reference signal (or clock). At least certain of the chips include an AC measurement circuit for comparing the periodicity of said reference signal with the periodicity of said on generated chip signal and cooperating with the delay regulator thereof to provide one of three discrete electrical manifestations.

IPC 1-7

G05F 1/46

IPC 8 full level

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