

Title (en)
Address buffer.

Title (de)
Adresspuffer.

Title (fr)
Mémoire tampon d'adresse.

Publication
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Application
EP 82301141 A 19820305

Priority
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Abstract (en)
An address buffer circuit for a dynamic memory comprises a flip-flop (FF), connected at one input/output terminal (N₁) with first input circuitry (IN₁) in parallel with third input circuitry (IN₃), and at its other input output terminal (N₂) with second input circuitry (IN₂) preferably in parallel with fourth input circuitry (IN₄). The second input circuitry receives a reference voltage (REF) and is activated by a timing clock (Ø_{ON}), during a normal operation mode. The first input circuitry is activated by an external address timing clock (Ø_{ON}) and receives an external address (ADD). The third input circuitry receives an internal refresh address (R) and is activated by an internal refresh address timing clock (Ø_{OR}). The address buffer (17) cooperates with a switcher which produces the internal refresh address timing clock (Ø_{OR}) and the external address timing clock (Ø_{ON}) alternatively, by switching a basic timing clock generated by an address drive clock generator. Such a circuit can enable higher operating speeds to be achieved.

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