

Title (en)
MEMORY DEVICE

Publication
EP 0062521 A3 19850710 (EN)

Application
EP 82301773 A 19820402

Priority
JP 4975681 A 19810402

Abstract (en)
[origin: EP0062521A2] A first-in-first-out memory device which is operable at a high-speed is disclosed. The memory device comprises a plural stages of memory units and a plural stages of control unit, each of the control units including means for indicating whether its stage holds effective data or not, means for receiving a signal of the indicating means of the previous stage, and means generating a write signal when the memory cell holds no effective data and the previous stage hold effective data, in which the write signal is used to remove data stored in the previous memory cell to the corresponding stage memory cell.

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G11C 19/00

IPC 8 full level
G06F 5/06 (2006.01); **G06F 5/08** (2006.01); **G11C 7/00** (2006.01); **G11C 19/00** (2006.01)

CPC (source: EP US)
G06F 5/08 (2013.01 - EP US); **G11C 19/00** (2013.01 - EP US)

Citation (search report)

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Designated contracting state (EPC)
DE FR GB

DOCDB simple family (publication)
EP 0062521 A2 19821013; EP 0062521 A3 19850710; EP 0062521 B1 19880803; DE 3278868 D1 19880908; JP S57164331 A 19821008; JP S6155688 B2 19861128; US 4459681 A 19840710

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