

Title (en)

METHOD OF MAKING A PLANAR III-V BIPOLAR TRANSISTOR BY SELECTIVE ION IMPLANTATION AND A DEVICE MADE THEREWITH.

Title (de)

VERFAHREN ZUR HERSTELLUNG EINES PLANAREN III-V-BIPOLAREN TRANSISTORS DURCH SELEKTIVE IONENIMPLANTATION UND NACH DIESEM VERFAHREN HERGESTELLTER TRANSISTOR.

Title (fr)

PROCEDE DE FABRICATION D'UN TRANSISTOR BIPOLAIRE III-V PAR IMPLANTATION SELECTIVE D'IONS ET DISPOSITIF OBTENU SELON CE PROCEDE.

Publication

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Application

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Priority

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Abstract (en)

[origin: WO8201619A1] A planar, bipolar transistor is fabricated by sequential selective area ion-implantation in III-V material, such as GaAs, to form two p-n junctions (16, 21). In an n-p-n device, an acceptor, e.g., Be, is implanted into an n-type collector region (11) supported by a substrate (10) to create a p-type base layer (15). The collector region may be epitaxially deposited on a highly doped substrate of the same conductivity type or, alternatively, ion-implanted in a region of a semi-insulating substrate. A donor implant, e.g., Si, is implanted within the base region to form at least one emitter region (20). The radiation damage is annealed out and the device is passivated, e.g., by a plasma-deposited silicon oxynitride dielectric layer (23), and appropriate ohmic contacts (24, 25, 26) to the emitter, base and collector regions are formed. The selective implant process uses evaporated masks of dense material and results in a truly planar device, which may be integrated on the same substrate with MESFET devices.

IPC 1-7

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IPC 8 full level

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CPC (source: EP US)

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- [A] FR 2358751 A1 19780210 - SIEMENS AG [DE]
- [A] ACTA ELECTRONICA, vol. 19, no. 2, April 1976 LIMEIL-BREVANNES (FR)

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