

Title (en)

APPARATUS FOR SIGNALLING THE END POINTS OF THE RAMP-DOWN INTERVAL IN A DUAL RAMP ANALOG TO DIGITAL CONVERTER

Publication

EP 0067109 A3 19851211 (EN)

Application

EP 82401033 A 19820608

Priority

US 27237181 A 19810610

Abstract (en)

[origin: EP0067109A2] In an integrated circuit type dual ramp analog to digital converter (10), the duration of the reference voltage integration, or ramp-down period, is precisely determined to control count accumulation in an external output counter (32a) operating in parallel with the standard internal counter of the integrated circuit. A reference voltage is stored on a flying capacitor (50) that is polarity switched, depending upon the polarity of the input signal, to be applied to the input of an integrator (12) during the ramp-down period. To establish the beginning and end of ramp-down, one end (52) of the flying capacitor (50) is applied to a comparator (54). As the voltage at the monitored end of the flying capacitor (50) undergoes abrupt level changes at the end points of the ramp-down interval, the comparator (54) generates start and stop pulses to the external output counter (32a).

IPC 1-7

H03K 13/20

IPC 8 full level

H03M 1/52 (2006.01); **H03M 1/00** (2006.01)

CPC (source: EP US)

H03M 1/52 (2013.01 - EP US)

Citation (search report)

[A] NEW ELECTRONICS, vol. 9, no. 5, March 09, 1976, pages 35,38,40,43, London, GB; L. EVANS et al.: "A low-cost, 4 1/2-digit A/D converter"

Designated contracting state (EPC)

AT DE FR GB IT NL SE

DOCDB simple family (publication)

EP 0067109 A2 19821215; **EP 0067109 A3 19851211**; JP S5812425 A 19830124; US 4383246 A 19830510

DOCDB simple family (application)

EP 82401033 A 19820608; JP 9993182 A 19820610; US 27237181 A 19810610