Title (en)

Single chip microcomputer.

Title (de)

Einchipmikrocomputer.

Title (fr)

Microprocesseur à pastille unique.

Publication

EP 0070458 A2 19830126 (EN)

Application

EP 82106083 A 19820707

Priority

JP 11185581 A 19810716

Abstract (en)

A single chip microcomputer comprising an instruction decoder (1) and function circuit (2) such as ROM, RAM, ALU, or the like, is further provided with parallel input shift register (4 or 12), which receives data of output terminals C1, C2...CN of the instruction decoder (1) at its respective stages in the corresponding order. Output signals of the shift register (4 or 12) are transferred to the external terminal (11) of to data bus (13) by means of gate means (9 or 15) upon receiving thereby of testing mode control signal from a testing mode control circuit (5). Thereby, by means of the testing mode control signal, the test output signal of the instruction decoder is issued to the external terminal only during the testing mode. By means of direct testing of the instruction decoder (1), the testing step is much simplified and testing time length is drastically shortened, thereby, production yield is improved and manufacturing cost is decreased.

IPC 1-7

G06F 11/26

IPC 8 full level

G06F 11/22 (2006.01); **G06F 11/267** (2006.01); **G06F 15/78** (2006.01)

CPC (source: EP)

G06F 11/2236 (2013.01)

Cited by

DE19718120C2; WO8606520A1

Designated contracting state (EPC)

DE FR GB

DOCDB simple family (publication)

EP 0070458 A2 19830126; **EP 0070458 A3 19850807**; CA 1187616 A 19850521; JP S5814265 A 19830127

DOCDB simple family (application)

EP 82106083 A 19820707; CA 407390 A 19820715; JP 11185581 A 19810716