Title (en)

ARRANGEMENT FOR THE AVOIDANCE OF FAULT IMPULSES OF A SUMMATION CURRENT TRANSFORMER

Publication

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Application

EP 82109160 A 19821004

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DE 3140866 A 19811014

Abstract (en)

[origin: EP0076999A2] The invention relates to an arrangement for the avoidance of fault impulses of a summation current transformer on its secondary winding (6). In such an arrangement, especially for fault-current protection switches, one lead (3, 4) surrounds the other (5) concentrically, in the region of the transformer core (2). By means of this arrangement, faulty disconnections are avoided, especially in the case of very high currents. <IMAGE>

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H01H 83/14

IPC 8 full level

H01H 83/14 (2006.01)

CPC (source: EP)

H01H 83/144 (2013.01); H01H 2083/146 (2013.01); H01H 2083/148 (2013.01)

Citation (search report)

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