Title (en)

SPLIT LOAD CIRCUIT.

Title (de)

SCHALTUNG MIT GETRENNTER LAST.

Title (fr)

CIRCUIT A CHARGE DIVISEE.

Publication

EP 0079884 A1 19830601 (EN)

Application

EP 81901777 A 19810526

Priority

US 8100698 W 19810526

Abstract (en)

[origin: WO8204364A1] A split load circuit (44) for driving a high speed load (72) and a low speed load (74) to the same logic state in response to one or more input signals. One input signal is provided to the gate terminals of pull-down transistors (48, 50, 52). The inverse of the input signal is provided to the gate terminals of pull-up transistors (64, 66). The high speed load (72) is connected between the pull-up transistor (64) and the pull-down transistor (50) and the low speed load (74) is connected between the pull-up transistor (66) and the pull-down transistor (52). When the input signal at the input node (46) is driven from one voltage state to another, the loads (72, 74) will be driven at different rates depending upon the capacitance and impedance of the load and the sizes of the pull-up transistors (64, 66) and the pull-down transistors (50, 52). The loads (72, 74) are driven independently such that much smaller pull-up and pull-down transistors can be utilized in place of a single pull-up and single pull-down transistor which would need to be fabricated much larger in order to meet the speed requirement of the high speed load (72) and to charge the high capacitance of the low speed load (74). Further, the power consumption is substantially reduced due to the reduced area of the transistors.

Abstract (fr)

Un circuit a charge divisee (44) sert a porter une charge a haute vitesse (72) et une charge a faible vitesse (74) au meme etat logique en reponse a un ou plusieurs signaux d'entree. Un signal d'entree est applique aux terminaux de portes des transistors de refoulement (48, 50, 52). L'inverse du signal d'entree est applique aux terminaux de portes des transistors de remontage (64, 66). La charge a haute vitesse (72) est connectee entre le transistor de remontage (64) et le transistor de refoulement (50) et la charge a faible vitesse (74) est connectee entre le transistor de remontage (66) et le transistor de refoulement (52). Lorsque le signal d'entree au point nodal d'entree (46) est porte d'un etat de tension a un autre, les charges (92, 74) sont transmises a des vitesses differentes en fonction de la capacitance et de l'impedance de la charge et des dimensions des transistors de remontage (64, 66) et des transistors de refoulement (50, 52). Les charges (72, 74) sont transmises independamment de maniere a pouvoir utiliser des transistors de remontage et de refoulement beaucoup plus petits a la place d'un transistor unique de remontage et d'un transistor unique de refoulement qui devraient autrement posseder des dimensions beaucoup plus grandes afin de satisfaire aux exigences de vitesse de la charge a vitesse elevee (72) et de charger la capacitance elevee de la charge a faible vitesse (74). La consommation de puissance se trouve en outre sensiblement reduite a la suite de la reduction de la surface des transistors.

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