

Title (en)  
INTEGRATED CURRENT SOURCE

Publication  
**EP 0080567 A3 19840404 (DE)**

Application  
**EP 82108273 A 19820908**

Priority  
DE 3136780 A 19810916

Abstract (en)  
[origin: EP0080567B1] 1. An integrated semiconductor current source circuit arrangement in the form of a current reflector comprising a plurality of output stages, each of which provides current to at least one load (R, L) and is in each case formed by a transistor stage (T2, T3, ..., Tn; T'3, ..., T'm), with a transistor stage (T1; T'1) to supply the output stages (T2, T3, ..., Tn; T'3, ..., T'm) with a control current (i1, ..., in), and a regulating circuit (OP, SG) provided to compare a signal (V1 - DELTA V), which represents the current (i0 +/- DELTA i) received from the control current supply transistor (T1; T'1), with a theoretical signal (Uref; Ur) supplied by a reference circuit (J0R, T1R; J0R, T1R, T2R; T1R, T2R, t1R, t2R), and form a comparison signal that regulates the control current supply transistor stage (T1; T'1), characterised in that the reference circuit (J0R, T1R; J0R, T1R, T2R; T1R, T2R, t1R, t2R) is a constant current source decoupled from the current reflector via the regulating circuit (OP, SG).

IPC 1-7  
**G05F 3/20**

IPC 8 full level  
**H03F 3/343** (2006.01); **G05F 3/20** (2006.01); **G05F 3/22** (2006.01); **G05F 3/26** (2006.01); **H01L 21/331** (2006.01); **H01L 21/8222** (2006.01); **H01L 27/082** (2006.01); **H01L 29/73** (2006.01); **H03F 3/34** (2006.01); **H03F 3/347** (2006.01)

CPC (source: EP US)  
**G05F 3/222** (2013.01 - EP US)

Citation (search report)

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**DE 3136780 A1 19830331**; DE 3277786 D1 19880114; EP 0080567 A2 19830608; EP 0080567 A3 19840404; EP 0080567 B1 19871202; JP S5866130 A 19830420; US 4965510 A 19901023

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**DE 3136780 A 19810916**; DE 3277786 T 19820908; EP 82108273 A 19820908; JP 16075982 A 19820914; US 29886889 A 19890117