

Title (en)
DIGITAL SIGNAL PROCESSOR

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Application
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Abstract (en)
[origin: EP0086570A2] A digital signal processor has timing means (5, 8) for providing a succession of sample intervals (ut) in which an incoming digital signals may have discrete values (e(o)). A serial delay (40, 52) such as a multi or single bit shift register progressively delays a digital signal giving a delayed signal (e(m)). An arithmetic section (36) has a plurality of elements (41, 54) such as multi or single bit multipliers, or difference squares. Each element operates on non delayed signals (e(o)) and signals (e(m)) from an associated stage of the delay (40, 52). An accumulating store (37) has a plurality of channels (45, 57) each associated with an arithmetic element (41, 54). Collectively the channels (45, 57) provide the required mathematical operation, auto or cross correlation function or structure function calculation. The interval of delay between channels (45, 57) is arranged to increase substantially geometrically e.g. by V2. The overall delay increase may be variable and geometric although increases between adjacent channels (45, 57) may be approximations to a geometric increase. A variable clip level circuit (53) may be incorporated into the input to the serial delay (52). In one configuration the delay intervals may be adjusted to be the same between each channel.

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G06F 15/336

IPC 8 full level
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• GB 1290336 A 19720927
• H.Z. Cummins and E.R. Pike, "Photon Correlation Spectroscopy and Velocimetry", Plenum Press 1977, pages 550-553
• J. Phys. A: Math. Gen., Vol 11, No. 9, 1978, The Institute of Physics, GB, pages 1729-1745.
• Applied Physics, 24, 1981, Springer Verlag, pages 323-329.

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