Title (en)

IMAGE DISPLAY MEMORY UNIT

Publication

EP 0093954 A3 19841003 (EN)

Application

EP 83104112 A 19830427

Priority

JP 7037382 A 19820428

Abstract (en)

[origin: EP0093954A2] An image display memory unit having a plurality of display memories (6, 7, 8) connected to a plurality of data lines of data bus (3) one for each display memory chip and addressable for each bit of the data bus comprises a display memory chip selection circuit (13) for selecting the display memory chip for each data bit on the same address, and a write control circuit (16, 17, 18) for controlling writing for each display memory. The dot-by-dot coloring is attained only by a software processing of controlling write information for each display memory and selecting the display memory chip.

IPC 1-7

G09G 1/28

IPC 8 full level

G06F 3/153 (2006.01); **G09G 5/00** (2006.01); **G09G 5/02** (2006.01); **G09G 5/39** (2006.01)

CPC (source: EP)

G09G 5/022 (2013.01)

Citation (search report)

- [A] US 4016544 A 19770405 - MORITA TAKAYA, et al
- [X] HEWLETT-PCKARD JOURNAL, vol. 31, no. 12, December 1980, pages 25-32, Amstelveen, NL; H.L. BAEVERSTAD et al.: "Display system designed for color graphics"

Cited by

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Designated contracting state (EPC)

DE GB

DOCDB simple family (publication)

EP 0093954 A2 19831116; **EP 0093954 A3 19841003**; JP S58187996 A 19831102

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EP 83104112 A 19830427; JP 7037382 A 19820428