Title (en)

COMPACT ROM WITH REDUCED ACCESS TIME

Publication

EP 0095847 B1 19901128 (EN)

Application

EP 83302747 A 19830516

Priority

US 38370982 A 19820601

Abstract (en)

[origin: EP0095847A2] The access time of a ROM circuit is reduced by isolating the relatively high impedance stack, formed of series connected driver transistors (TI min ,...TN min), from a relatively high capacitive pre-charged output (14). An isolation transistor (Ti) has its control terminal connected to the stack through a control node (10 min) and its output circuit connected between the output node (14) and ground. A switched ground technique is used to charge the control node (10 min) prior to addressing. During read-out, if any of the series connected driver transistors in the stack are not rendered conductive, due to the level of the address signals applied thereto, the control node remains charged, causing the isolation transistor (Ti) to remain conductive and the output node is thus discharged.

IPC 1-7

G11C 17/12

IPC 8 full level

G11C 17/00 (2006.01); **G11C 17/12** (2006.01); **G11C 17/18** (2006.01)

CPC (source: EP US)

G11C 17/123 (2013.01 - EP US)

Citation (examination)

JP S53125787 A 19781102 - NIPPON ELECTRIC CO

Cited by

GB2170671A; GB2170671B

Designated contracting state (EPC)

CH DE FR GB IT LI NL

DOCDB simple family (publication)

EP 0095847 A2 19831207; **EP 0095847 A3 19851009**; **EP 0095847 B1 19901128**; DE 3382017 D1 19910110; JP S58218100 A 19831219; US 4480320 A 19841030

DOCDB simple family (application)

EP 83302747 A 19830516; DE 3382017 T 19830516; JP 9587683 A 19830601; US 38370982 A 19820601