

Title (en)
Gate-array chip.

Title (de)
Gattermatrixchip.

Title (fr)
Puce comprenant une matrice de portes.

Publication
EP 0098163 A2 19840111 (EN)

Application
EP 83303760 A 19830629

Priority
JP 11152982 A 19820630

Abstract (en)
A gate-array chip comprises a plurality of basic-cell arrays (40) arranged parallel to one another on a semiconductor bulk (60), and a plurality of impurity regions (50) formed on the semiconductor bulk and in regions between the basic-cell arrays. The impurity regions and part of the basic-cell arrays are adapted to form input/output circuits (10) whereby the gate-array chip can be divided into several chips each having a desired size and a desired number of gates.

IPC 1-7
H01L 27/02

IPC 8 full level
H01L 21/822 (2006.01); **H01L 21/82** (2006.01); **H01L 27/04** (2006.01); **H01L 27/118** (2006.01); **H03K 5/02** (2006.01); **H03K 19/094** (2006.01); **H03K 19/0948** (2006.01); **H03K 19/177** (2006.01)

CPC (source: EP US)
H01L 21/82 (2013.01 - EP US); **H01L 27/11807** (2013.01 - EP US); **H03K 5/023** (2013.01 - EP US); **H03K 19/09425** (2013.01 - EP US); **H03K 19/09429** (2013.01 - EP US); **H03K 19/0948** (2013.01 - EP US); **H03K 19/17704** (2013.01 - EP US); **H03K 19/17728** (2013.01 - EP US); **H03K 19/17744** (2013.01 - EP US); **H03K 19/17796** (2013.01 - EP US); **H01L 2924/0002** (2013.01 - EP US)

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DE FR GB

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US 4733288 A 19880322; DE 3380507 D1 19891005; EP 0098163 A2 19840111; EP 0098163 A3 19860416; EP 0098163 B1 19890830; JP H0114707 B2 19890314; JP S593950 A 19840110

DOCDB simple family (application)
US 82809786 A 19860210; DE 3380507 T 19830629; EP 83303760 A 19830629; JP 11152982 A 19820630