

Title (en)
INTEGRATED CIRCUIT CONTACT FABRICATION PROCESS

Publication
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Application
EP 83902867 A 19830816

Priority
US 40919382 A 19820818

Abstract (en)
[origin: WO8400850A1] A process for fabricating an electrical contact which connects an epitaxial layer (2), well, or substrate with a metallic interconnect layer (62) during the course of creating active integrated circuit devices (16, 17) in a semiconductor wafer. The process forms a self-aligned contact by establishing the contact location (14) coincident with the definition of the active regions in the wafer, at an early step in the wafer fabrication process. Thereafter, a gate silicon dioxide layer (21) and a polycrystalline silicon electrode layer (37) are combined to mask the contact region surface from intermediate process environments, e.g., ion implantation and POCl₃ diffusion operations. As the integrated circuit fabrication process approaches conclusion, the contact region (14) is opened by a selective etch of the polycrystalline silicone (37) and the silicon dioxide (21) layers, an enhancement implant into the surface of the contact region, a hydrogen environment annealing operation, and a deposition and patterning of the metallic interconnect layer (62).

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H01L 21/60

IPC 8 full level
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