

Title (en)

SYNCHRONISATION DEVICE FOR A FRAME-STRUCTURED DIGITAL TRANSMISSION, AND RECEIVER CONTAINING SUCH A DEVICE

Publication

EP 0133081 B1 19881005 (FR)

Application

EP 84401411 A 19840703

Priority

FR 8311614 A 19830712

Abstract (en)

[origin: US4594728A] A synchronization device for digital data frame transmission system comprising an n bit series register transferring its contents at the line frequency to a parallel register also of n bits. The m first bits of the series register are also directed to a logic circuit which tests their conformity with the beginning of the synchronization word. When there is conformity, the logic circuit controls a divider dividing by n which controls, in its turn, at the line frequency divided by n, the transfer of the contents of the parallel register to a PROM memory. The purpose of the PROM is to recognize the entire synchronization word. When there is no recognition, the operation of the divide by n divider is inhibited and the procedure begins again.

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H04J 3/06

IPC 8 full level

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CPC (source: EP US)

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