

Title (en)
IGNITION TIMING CONTROL DEVICE FOR A TEST BED

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Application
EP 84109698 A 19840815

Priority
DE 3336917 A 19831011

Abstract (en)
[origin: EP0137229A2] 1. Ignition timing control apparatus for an engine test bed, for generating ignition pulses of adjustable ignition timing with respect to a reference angle, counting pulses and a reference pulse being derived from a toothed ring coupled to the crankshaft, characterized by the following features : a) a shaping circuit (1) serves for separating the counting pulses from the reference pulse sequence and for doubling and quadrupling the counting pulses ; b) adjustment devices (9, 8) are provided for setting the ignition timing as an ignition value corresponding to a number of counting pulses before the reference angle and for inputting the number of teeth of the toothed ring ; c) coupled to the adjustment device (9, 8) is a calculator circuit (10) for calculating the number of ignition timing pulses as the difference between the number of teeth and the ignition value, the calculator circuit (10) providing in two holding stages (11, 12) on the one hand the number of teeth and on the other hand the number of ignition timing pulses ; d) a first counter (6) is coupled to the output of the shaping circuit (1) on which the number of counting pulses is doubled ; e) the reference pulse line (3) is connected to the reset input of the first counter and to the holding stage (11) for the number of ignition timing pulses of the calculator circuit (10) ; f) the output of the first counter (6) is connected to the holding stage (12) for the number of teeth of the calculator circuit (10) ; g) both holding stages (11, 12) are connected to the preload input of the first counter (6) ; h) a D flipflop (17) is connected by means of its clock input (19) to the output of the first counter (6) ; j) an inverting output (23) of the D flipflop (17) leads back to the data input (24) ; k) two groups of transistor ignition stages (25, 27 and 26, 28) are connected on the one hand to the outputs (20, 23) and on the other hand to the inverting outputs (21, 23) of the D flipflop (17).

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