Title (en)

GRAPHIC DISPLAY CONTROLLER

Publication

EP 0149399 B1 19880727 (FR)

Application

EP 84402739 A 19841227

Priority

FR 8400355 A 19840111

Abstract (en)

[origin: EP0149399A2] 1. A graphic visualization controller comprising a command processor, a bilateral interface exchange circuit with a control microprocessor and output interface circuit controlled by the command processor and connected with a graphic visualization device and an associated screen memory constituted by a plurality of memory planes intended for storing an image in its different aspects of display, respectively, and in which the said output interface circuits comprise means for generating a video sync signal, a signal termed the memory sequence formed by image refresh cycles for displaying same and data modification cycles for the modification of the stored image and an address signal for the said screen for reading and writing image data words and a data switch connected to the said screen memory in order to ensure a modification of the stored image at the address defined by the address signal in the course of each data modification cycle, characterized in that the said data switch comprises ; - a generator (12) for the data image fictive word, termed the transposition word, whose respective bits are of the same value, - a plurality of data correction devices (3A - 3D) each connected on the one hand with one of the memory planes (3A - 3D) for which it is intended, in order to receive a read data word from this memory plane and to supply it with a modified data word, and on the other hand with the control microprocessor (1) in order to receive an operational mode command signal, - and a direction circuit (11) coupling the said transposition word generator (12) with the said command processor (5) and delivering in reply on an output bus (23) connected jointly with the said correcting devices, a word termed the mask word defining positionally, in the data words received by the different correcting devices of the respective memory plane, at least one of the bits to be modified.

IPC 1-7

G09G 1/16; G09G 1/28

IPC 8 full level

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CPC (source: EP)

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