Title (en)

A BYTE WIDE MEMORY CIRCUIT HAVING A COLUMN REDUNDANCY CIRCUIT.

Title (de)

BYTE-ORGANISIERTE SPEICHERANORDNUNG MIT EINER SPALTENREDUNDANZ-SCHALTUNG.

Title (fr)

CIRCUIT DE MEMOIRE PAR QUARTETS AYANT UN CIRCUIT DE REDONDANCE DE COLONNES.

Publication

EP 0150194 A4 19880426 (EN)

Application

EP 84902271 A 19840517

Priority

US 51420383 A 19830714

Abstract (en)

[origin: WO8500460A1] A 4-bit byte wide memory circuit (12) having a column redundancy scheme including a plurality of bit segments (BS), each having columns (18, 20), for storing data, a plurality of data lines (DL), corresponding, respectively, to the plurality of bit segments (BS), a plurality of I/O ports (PM) coupled, respectively, to the plurality of data lines (DL), a plurality of redundant columns (RC) for storing data and corresponding, respectively, to the plurality of I/O ports (PM), and a programmable circuit (28) for coupling, respectively, the plurality of redundant columns (RC) to one or another of the data lines (DL) while decoupling the bit segments (BS) from the data lines (DL).

IPC 1-7

G11C 7/00

IPC 8 full level

G11C 29/00 (2006.01); **G11C 29/04** (2006.01)

CPC (source: EP)

G11C 29/846 (2013.01)

Citation (search report)

- [X] WO 8102360 A1 19810820 - MOSTEK CORP [US]
- [X] EP 0044628 A2 19820127 - INMOS CORP [US]
- See references of WO 8500460A1

Designated contracting state (EPC)

AT BE CH DE FR GB LI LU NL SE

DOCDB simple family (publication)

WO 8500460 A1 19850131; EP 0150194 A1 19850807; EP 0150194 A4 19880426; JP S60501878 A 19851031

DOCDB simple family (application)

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