Title (en)

SHALLOW-JUNCTION SEMICONDUCTOR DEVICES.

Title (de)

HALBLEITERANORDNUNG MIT UNTIEFEM ÜBERGANG.

Title (fr)

DISPOSITIF SEMI-CONDUCTEUR A JONCTION PEU PROFONDE.

Publication

EP 0151585 A4 19860220 (EN)

Application

EP 84902405 A 19840604

Priority

US 51675583 A 19830725

Abstract (en)

[origin: WO8500694A1] A shallow-junction semiconductor device is fabricated by initially implanting a neutral species (non-doping impurity) into a surface region (30, 32) of a semiconductor body (10) prior to the introduction of a dopant therein. This implant serves as a getter for defects and also as a physical barrier. The thermal diffusivity of subsequently introduced dopant species is thereby significantly reduced. As a result, extremely shallow junctions (36, 38) are realized.

IPC 1-7

H01L 21/265; H01L 21/94; H01L 29/06; H01L 29/32; H01L 29/78

IPC 8 full level

H01L 29/78 (2006.01); **H01L 21/225** (2006.01); **H01L 21/265** (2006.01); **H01L 21/322** (2006.01); **H01L 29/167** (2006.01)

CPC (source: EP US)

H01L 21/2253 (2013.01 - EP); **H01L 21/26506** (2013.01 - EP US); **H01L 21/26513** (2013.01 - EP US); **H01L 29/167** (2013.01 - EP)

Citation (search report)

- [A] DE 2014797 A1 19701008
- [X] JOURNAL OF THE ELECTROCHEMICAL SOCIETY, vol. 116, no. 1, January 1969, pages 73-77, Princeton, US; T.H. YEH et al.: "Strain compensation in silicon by diffused impurities"
- [A] IBM TECHNICAL DISCLOSURE BULLETIN, vol. 21, no. 8, January 1979, pages 3154-3156, New York, US; W.K. CHU et al.: "Method of reducing arsenic thermal diffusion by noble gas ion implantation"
- See references of WO 8500694A1

Designated contracting state (EPC)

BE DE FR GB NL

DOCDB simple family (publication)

WO 8500694 A1 19850214; CA 1222835 A 19870609; EP 0151585 A1 19850821; EP 0151585 A4 19860220; JP S60501927 A 19851107

DOCDB simple family (application)

US 8400851 W 19840604; CA 457570 A 19840627; EP 84902405 A 19840604; JP 50239784 A 19840604