Title (en)
ULTRA-RAPID TIME-NUMERICAL CONVERTER

Publication
EP 0165108 B1 19890322 (FR)

Application
EP 85400870 A 19850506

Priority
FR 8407344 A 19840511

Abstract (en)
[origin: US4719608A] A chain of gates is formed on one and the same substrate of integrated circuit to enable the propagation along the chain of a starting signal received at one end of the chain, and a locking circuit formed for example by another chain of gates has outputs connected to the gates of the chain in order to be able to block the state thereof following the reception of a stop signal, so that the number of gates gone through by the starting signal is a linear function of the time elapsed between the reception of the starting signal and the reception of the stop signal.

IPC 1-7
G04F 10/00; H03M 1/50

IPC 8 full level
H03M 1/50 (2006.01); **G04F 10/00** (2006.01); **G04F 10/04** (2006.01); **H03M 1/00** (2006.01)

CPC (source: EP US)
G04F 10/00 (2013.01 - EP US); **G04F 10/005** (2013.01 - EP US)

Cited by
EP0508232A3

Designated contracting state (EPC)
AT BE CH DE FR GB IT LI LU NL SE

DOCDB simple family (publication)
EP 0165108 A1 19851218; **EP 0165108 B1 19890322**; AT E41713 T1 19890415; DE 3569049 D1 19890427; FR 2564216 A1 19851115; FR 2564216 B1 19861024; JP S60253994 A 19851214; US 4719608 A 19880112

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EP 85400870 A 19850506; AT 85400870 T 19850506; DE 3569049 T 19850506; FR 8407344 A 19840511; JP 9813885 A 19850510; US 73239285 A 19850509