Title (en)

INTERFACE CIRCUIT OF THE SLAVE TYPE WORKING WITH A SERIAL BUS

Publication

EP 0168077 B1 19890524 (FR)

Application

EP 85200879 A 19850605

Priority

FR 8409064 A 19840608

Abstract (en)

[origin: US4695839A] A slave-type interface circuit operating with a series bus in a configuration in which writing takes place after recognition of an address. A cycle transmitted by the bus contains an address sequence and a data sequence. The circuit controls a plurality of user circuits (COM) on the basis of data stored in a memory (M) and of a decoder (CDEC). A register (REG) and a bus logic (BUSL) receive at their inputs (L1, L2) information (SDA) and clock (SCL) signals. The bus logic (BUSL) receives from an identification circuit (AIC) a signal (DVA) indicating whether or not the address transmitted by the bus corresponds to an address A0, A1, A2 displayed at the inputs S0, S1 and S2. It controls the circuit on the basis of the register (REG) initialization signal (RST1), a signal LDS) for the authorization of the loading of data into the memory (M) and an acceptance signal (ACK) transmitted in the direction of the bus.

IPC 1-7

G06F 13/42

IPC 8 full level

G06F 13/36 (2006.01); **G06F 13/16** (2006.01); **G06F 13/20** (2006.01); **G06F 13/38** (2006.01); **G06F 13/42** (2006.01); **H04Q 9/00** (2006.01)

CPC (source: EP KR US)

G06F 13/00 (2013.01 - KR); **G06F 13/4291** (2013.01 - EP US)

Cited by

EP0604309A1; FR2699707A1; WO9415296A1

Designated contracting state (EPC)

DE FR GB IT

DOCDB simple family (publication)

EP 0168077 A1 19860115; **EP 0168077 B1 19890524**; CA 1229419 A 19871117; DE 3570536 D1 19890629; FR 2565752 A1 19851213; FR 2565752 B1 19860905; JP H0816896 B2 19960221; JP S616752 A 19860113; KR 860000597 A 19860129; KR 920009436 B1 19921016; US 4695839 A 19870922

DOCDB simple family (application)

EP 85200879 A 19850605; CA 483310 A 19850606; DE 3570536 T 19850605; FR 8409064 A 19840608; JP 12283385 A 19850607; KR 850003970 A 19850607; US 74109085 A 19850604