Title (en)

FRAME SYNCHRONISATION DEVICE

Publication

EP 0171789 B1 19890809 (FR)

Application

EP 85110127 A 19850813

Priority

- FR 8412915 A 19840817
- FR 8419175 A 19841214

Abstract (en)

[origin: US4675886A] Frame synchronization devices utilize a frame alignment word decoder connected to the outputs of a shift register which receives on its input the received data bit stream. It is clocked by a clock signal generated from a selection of periods of the data bit stream timing signal reproducing a periodic pattern. This pattern is formed by relative bit locations within the duration of a frame certain at least of which are distributed according to the distribution of the bits of an alignment word in a frame and which form groups of the same size regularly distributed over the duration of a frame. This clock signal is generated in the device by a divider which divides by 20 or by 21 which imposes on it a periodic phase skip by the value of one period of the data bit stream timing for as long as the alignment word is not recognized by the decoder. The shift register is implemented in two parallel parts clocked by versions of the clock signal with a relative phase shift between them, one of which parts updates the other part in parallel on each phase skip of the clock signal.

IPC 1-7

H04J 3/06

IPC 8 full level

H04J 3/06 (2006.01)

CPC (source: EP US)

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Cited by

EP0320882A3; AU624407B2; EP0652656A1; FR2712446A1; US5625654A; EP0258893A3

Designated contracting state (EPC)

BE DE FR GB IT LU NL

DOCDB simple family (publication)

EP 0171789 A1 19860219; **EP 0171789 B1 19890809**; CA 1240061 A 19880802; DE 3572277 D1 19890914; DK 373485 A 19860218; DK 373485 D0 19850816; IE 56693 B1 19911106; IE 852018 L 19860217; US 4675886 A 19870623

DOCDB simple family (application)

EP 85110127 A 19850813; CA 488844 A 19850816; DE 3572277 T 19850813; DK 373485 A 19850816; IE 201885 A 19850816; US 76701785 A 19850819