

Title (en)

WAFER SCALE PACKAGE SYSTEM AND HEADER AND METHOD OF MANUFACTURE THEREOF.

Title (de)

PACKUNGSSYSTEM AUF HALBLEITERSCHEIBENSKALA UND LEITER UND VERFAHREN ZUM HERSTELLEN DERSELBEN.

Title (fr)

SYSTEME DE BOITIER A L'ECHELLE DE LA TRANCHE, BARRETTE, ET PROCEDE DE FABRICATION.

Publication

EP 0174950 A4 19880205 (EN)

Application

EP 85901256 A 19850221

Priority

US 58197584 A 19840221

Abstract (en)

[origin: WO8503804A1] Wafer scale device (10, 201) on which is formed a layer of thin film as an interconnection system (203) with contact sites (202, 207) between the interconnection system (203) and die bonding sites (202) of the wafer (10, 201) to form a monolithic wafer. The interconnection system (203) has bonding sites on the surface of the wafer (10, 201) to which chips (11) are bonded to form a hybrid monolithic wafer system. The wafer (10) is packaged within a wafer package, (Fig. 4), and the packaging system utilizes a header (20) which is a flexible circuit connector between the wafer package and first level circuit board (30).

IPC 1-7

H01L 23/12; **H01L 23/32**; **H01L 23/48**; **H01L 27/10**

IPC 8 full level

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CPC (source: EP)

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C-Set (source: EP)

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5. **H01L 2924/12033** + **H01L 2924/00**
6. **H01L 2924/14** + **H01L 2924/00**

Citation (search report)

- WO 8202640 A1 19820805 - JOHNSON ROBERT ROYCE [US], et al
- WO 8202603 A1 19820805 - JOHNSON ROBERT ROYCE [US]
- 32nd Electronic Components Conference, May 10-12, 1982, San Diego, pages 7-16, IEEE, New York, US; Y. HSIA et al.: "A reconfigurable interconnect for in-silicon electronic assembly", page 8: "Empirical examination of basic concepts"; figures 3-5.
- See references of WO 8503804A1

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