Title (en)
TIMING RECOVERY CIRCUIT FOR MANCHESTER CODED DATA

Publication
EP 0178622 B1 19890315 (EN)

Application
EP 85113025 A 19851014

Priority
JP 21583184 A 19841015

Abstract (en)
[origin: US4661965A] A timing recovery circuit for recovering timing signals out of split phase or Manchester coded data, comprising dotting (DOT), frame synchronization (FS) and information (DATA) in digital form. A digital voltage controlled oscillator (VCO) provides a signal whose frequency is twice that of the timing signal of the split phase signal and a frequency divider generates a signal whose frequency is equal that of the timing signal. The outputs of the VCO and the frequency divider are selectively applied to a phase detector, also having as an input the split phase signal, for the generation of a feedback control signal, depending on whether the split phase signal is advanced or delayed. The higher-frequency VCO signal is applied during the DATA segment of the incoming signal while the frequency divider signal is applied during the DOT and FS segments.

IPC 1-7
H04L 7/02; H04L 7/10; H04L 25/49

IPC 8 full level
H04L 7/00 (2006.01); **H04L 7/033** (2006.01); **H04L 7/04** (2006.01); **H04L 7/10** (2006.01); **H04L 25/49** (2006.01)

CPC (source: EP US)
H04L 7/046 (2013.01 - EP US); **H04L 7/10** (2013.01 - EP US); **H04L 25/4904** (2013.01 - EP US); H04L 7/033 (2013.01 - EP US)

Cited by
DE19813965C1; EP0492704A1; GB2200518A; EP0282202A3; US6249558B1

Designated contracting state (EPC)
DE FR GB NL SE

DOCDB simple family (publication)
US 4661965 A 19870428; AU 4870885 A 19860424; AU 575207 B2 19880721; CA 1242029 A 19880913; DE 3568925 D1 19890420; EP 0178622 A2 19860423; EP 0178622 A3 19861008; EP 0178622 B1 19890315; HK 19591 A 19910322; JP H0546730 B2 19930714; JP S6194429 A 19860513; SG 8791 G 19910405

DOCDB simple family (application)
US 78741985 A 19851015; AU 4870885 A 19851015; CA 492859 A 19851011; DE 3568925 T 19851014; EP 85113025 A 19851014; HK 19591 A 19910314; JP 21583184 A 19841015; SG 8791 A 19910218