Title (en)

ANNUNCIATOR IDENTIFICATION ARRANGEMENT IN AN ALARM SYSTEM

Publication

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Application

EP 85111427 A 19850910

Priority

DE 3433476 A 19840912

Abstract (en)

[origin: EP0179248A1] 1. Annunciator identification arrangement in an alarm system, especially a fire alarm system, having several two-wire annunciation circuits (ML), which are monitored on closed circuit and are connected to an evaluation device (AWE) at a control centre (Z) and to which several annunciators (M1, M2,...) are connected in each case, an alarm-triggering annunciator causing a voltage dip in the line voltage (UL) concerned by virtue of limiting the line current (IL) from the control centre to a first current limiting voltage, and an alarm annunciation of the annunciation circuit (ML) concerned being derived therefrom in the control centre (Z), and the control centre (Z) sending current pulses (IPZ) with a second, increased current limiting value to the annunciation circuit (ML) concerned, the alarm-triggering annunciator causing an increased current flow on the annunciation circuit, characterized in that an annunciator supplementary circuit arrangement (MZS) is assigned to each annunciator (M1, M2,...) and together with the annunciator composes an annunciator unit (ME1, ME2,...), in that the annunciator suplementary circuit arrangement (LZS) has an annunciator display (MA) connected to the annunciator circuit (ML) via a controllable switching element (TR1), a pulse divider (IPT) to which the current pulses (IPZ) are applied, and the divider ratio of which can be adjusted by means of switches (S1-Sn) in order to form an annunciator address, and a current reducing device (SRE) arranged in the annunciator connecting branch (1-a) and capable of being triggered by the pulse divider (IPT), the annunciator display (MA) of the alarm-triggering annunciator being switched in with each current pulse (IPZ), and the pulse divider (IPT) being switched further into its original state with the first current pulse (IPZ) and as far as its preset value with each further current pulse (IPZ), and the pulse divider (IPT) further delivering a control signal to the current reducing device (SRE) upon reaching its preset value, and in that there is arranged in the control centre (Z) of the evaluation device (AWE) an annunciator identification circuit arrangement (MIS), which has a current measuring device (SME) for monitoring the line current (IL), an analog-digital converter (AD), to the first input (E) of which the measured line current is applied, and a microcomputer (MR) downstream of the analog-digital converter (AD) with a display device (ANZ) for the annunciator address, the digitised current values being fed from the output (QW) of the analog-digital converter (AD) to the microcomputer (MR), which is connected with a further input (F) of the analog-digital converter (AD) on the one hand, and to which are applied the current pulses (IPZ) of the increased line current (flashing rate), on the other hand, it being the case, further, that the current pulses (IPZ) are counted up to the current-reduced pulse and the address of the alarm-triggering annunciator is derived therefrom and displayed.

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G08B 25/00; G08B 26/00

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