

Title (en)

Cache memory addressable by both physical and virtual addresses.

Title (de)

Durch beide, physikalische und virtuelle Addressen, addressierbarer Cache-Speicher.

Title (fr)

Antémémoire adressable par les deux adresses physiques et virtuelles.

Publication

**EP 0180369 A2 19860507 (EN)**

Application

**EP 85307393 A 19851015**

Priority

US 66685384 A 19841031

Abstract (en)

A cache memory addressable by both physical and virtual addresses includes a cache data memory (64) and a tag memory (66). The tag memory (66) is comprised of a virtual tag memory (68) and a physical tag memory (70). The physical and virtual tag memories are both addressable by the least significant bits (LSB) of the address signal to output tag portions of addresses associated with data stored in the cache data memory (64). A switch (78) selects between the outputs from the memories (68) and (70) under control of an arbitration unit (88). The arbitration unit (88) distinguishes between virtual or physical addresses input thereto. A comparator (100) compares the selected tag portion with the tag portion of the received address to determine if a match exists. If a match exists, the output of the cache data memory is selected with a switch (84).

IPC 1-7

**G06F 12/08**

IPC 8 full level

**G06F 12/08** (2006.01); **G06F 12/0864** (2016.01); **G06F 12/10** (2006.01); **G06F 12/1045** (2016.01); **G06F 12/12** (2006.01); **G06F 12/126** (2016.01)

CPC (source: EP)

**G06F 12/0864** (2013.01); **G06F 12/1045** (2013.01); **G06F 12/126** (2013.01)

Cited by

EP0394502A1; GB2260429A; GB2260429B; GB2297398A; US5717892A; GB2297398B; EP0706133A3; US5640534A; EP0708404A3; US5805855A; FR2619641A1; WO9000283A1

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