Title (en)

FRAME BUFFER MEMORY CONTROLLER

Publication

EP 0192139 A3 19900425 (EN)

Application

EP 86101598 A 19860207

Priority

US 70298285 A 19850219

Abstract (en)

[origin: EP0192139A2] A frame buffer memory controller (24) allows rapid image updating while maintaining screen refresh data flow rate. One frame buffer memory controller (24) controls one or more pixel depth columns comprising one or more frame buffer memory chips (22) per pixel. Each frame buffer memory controller (24) listens on a display processor bus (26) for read, write or read-modify-write commands addressed to a pixel, or memory chip, under its control. Such commands, along with the associated addresses and data, are stored in a first-in, first-out (FIFO) buffer (35) for execution during the first free memory cycle.

IPC 1-7

G09G 1/16

IPC 8 full level

G09G 5/395 (2006.01); **G01R 13/20** (2006.01); **G09G 5/00** (2006.01); **G09G 5/36** (2006.01); **G09G 5/39** (2006.01)

CPC (source: EP)

G09G 5/39 (2013.01)

Citation (search report)

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- [A] US 4092728 A 19780530 - BALTZER PHILIP KEENE
- [A] US 4150364 A 19790417 - BALTZER PHILIP K
- [A] ELECTRONIC DESIGN, vol. 32, no. 14, July 1984, pages 135-142, Waseca, MN, Denville, NJ, US; H. ASSARPOUR: "Graphics controller chip raises video data rate, is simpler to program"

Cited by

CN109410828A; EP0284905A3; US5731811A; EP0279228A3; EP0618560A1; EP0563855A3; US5539873A

Designated contracting state (EPC)

DE FR GB NL

DOCDB simple family (publication)

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DOCDB simple family (application)

EP 86101598 A 19860207; CA 502050 A 19860218; JP 3494086 A 19860219