Title (en)
DISPLAY CONTROLLER

Publication
EP 0195998 A3 19881005 (EN)

Application
EP 86103631 A 19860318

Priority
- JP 5660385 A 19850320
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Abstract (en)
[origin: EP0195998A2] A display controller (10) controls an aspect ratio of an image displayed on a screen of a scanning type display device (12). A horizontal counter (13) counts a clock pulse (CP) to output column address data for a video RAM (V-RAM) (11), and a vertical counter (14) counts a decoded signal of the column address data to generate row address data for the V-RAM (11). Each time the row address data becomes equal to a predetermined value, a correction circuit (17) prevent the decoded signal from being supplied to the vertical counter (14) for a time interval corresponding to one horizontal scanning line, whereby an additional horizontal scanning line is displayed with the same image data as the horizontal scanning line displayed immediately before. Vertical lines can also be added in the similar manner to control an aspect ratio of the displayed image.

IPC 1-7
G09G 1/16

IPC 8 full level
G09G 5/18 (2006.01); **G09G 5/391** (2006.01)

CPC (source: EP)
G09G 5/18 (2013.01); **G09G 5/391** (2013.01); G09G 2340/0442 (2013.01)

Citation (search report)
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EP0465063A3; US5633655A

Designated contracting state (EPC)
DE GB NL

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