

Title (en)
PROCESS FOR FABRICATING A SELF-ALIGNED BIPOLAR TRANSISTOR

Publication
EP 0199497 B1 19920102 (EN)

Application
EP 86302631 A 19860409

Priority
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Abstract (en)
[origin: EP0199497A2] Using a single mask pattern (36,37) on a semiconductor substrate (31), a doped base contact region (39) adjacent the surface of the substrate, a buried insulating region (38) below the base contact region, and an insulating layer (40) on the base contact region are formed. Optionally, a metal or metal silicide base-electrode-taking-out is formed on the base contact region. Doped emitter (44) and intrinsic base (41) regions are formed below the mask pattern. A collector region (33) is defined by the base contact region and the buried insulating layer to be therebetween i.e. below the mask pattern. Hence, the bipolar transistor formed thereby has a size which is no larger than necessary, thereby reducing the collector-base capacitance, the base resistance, and the size of the device.

IPC 1-7
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IPC 8 full level
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CPC (source: EP KR US)
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Cited by
EP0326211A1; GB2243716B; GB2243716A; US5159423A; GB2223126A; GB2223126B; WO2006114746A3

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