Title (en)

ROW PROCESSOR FOR BIT-MAP DISPLAY

Publication

EP 0201267 A3 19900404 (EN)

Application

EP 86303243 A 19860429

Priority

US 73000385 A 19850502

Abstract (en)

[origin: EP0201267A2] A row processor unit for a bit-map, raster scan display performs per-scan-line frame buffer management functions. A portion of the frame buffer memory which is not used for display contains load/decode parameters. These parameters are accessed by the row processor unit during the horizontal blanking interval and used for display and data movement operations during the refreshing of the following scan line. A pattern memory provides pixel masks for scrolling as well as providing cursor patterns.

IPC 1-7

G09G 1/16

IPC 8 full level

G09G 5/36 (2006.01); **G09G 5/08** (2006.01); **G09G 5/34** (2006.01); **G09G 5/39** (2006.01)

CPC (source: EP)

G09G 5/08 (2013.01); **G09G 5/346** (2013.01)

Citation (search report)

- [A] FR 2544898 A1 19841026 - TEXAS INSTRUMENTS FRANCE [FR]
- [A] EP 0058011 A2 19820818 - SYNTREX INC [US]
- [A] E.D.N. ELECTRICAL DESIGN NEWS, vol. 29, no. 11, May 1984, pages 153-170, Boston, Massachusetts, US; M.S. YOUNG: "Use a CRT-controller chip to mix text and graphics"

Cited by

US4987551A; AU611521B2; WO8906030A1

Designated contracting state (EPC)

DE FR GB NL

DOCDB simple family (publication)

EP 0201267 A2 19861112; **EP 0201267 A3 19900404**; JP S61254984 A 19861112

DOCDB simple family (application)

EP 86303243 A 19860429; JP 9930586 A 19860428