

Title (en)  
METHOD FOR FABRICATING MODULES COMPRISING STACKED CIRCUIT-CARRYING LAYERS

Publication  
**EP 0204767 B1 19910227 (EN)**

Application  
**EP 85906123 A 19851120**

Priority  
US 67409684 A 19841123

Abstract (en)  
[origin: WO8603338A1] A method and related fixtures which permit formation of stacks of thin circuitry-carrying layers. The layers terminate in an access plane having a two-dimensional array of closely-spaced electrical leads. The method includes the steps of measuring the thickness of separate chips, selecting groups of chips having appropriate thicknesses, applying appropriate amounts of epoxy between adjacent chips, aligning the chips (and their electrical leads) in the direction parallel to their planes (i.e., the X-axis), and closing the cavity with an end wall which (a) exerts pressure on the stacked chips and epoxy in a direction perpendicular to the chip planes, and (b) establishes a fixed height of the stack in order to align the leads in the Y-axis. The final fixture provides a fixed-size cavity for confining the layers during curing of thermo-setting adhesive which has been applied between each adjacent pair of layers. An initial fixture is provided for accurately measuring the thickness of each layer under substantial layer-flattening pressure. An intermediate fixture is provided for wet stacking the layers prior to their insertion into the final fixture.

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IPC 8 full level  
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