

Title (en)

TEST METHOD FOR DETECTING FAULTY MEMORY CELLS IN A PROGRAMMABLE SEMICONDUCTOR DEVICE

Publication

**EP 0214914 B1 19911204 (EN)**

Application

**EP 86401968 A 19860909**

Priority

JP 19876185 A 19850909

Abstract (en)

[origin: EP0214914A2] For testing unwritten-in field programmable memory cells, after some specified written-in cells have been previously provided in the semiconductor device, the method comprises: enabling a readout circuit (READOUT) which reads datum written in the memory cell; switching addressing-signals selecting the memory cell from a written-in cell ( $M_{\text{sub}t}$ ) to an unwritten-in cell ( $M_0, M_1, \dots$ ) to be tested, causing the voltage of the bit line operatively connected to the selected unwritten-in cell to start to rise gradually to that of the unwritten-in cell; and detecting the delay of this rising voltage after the moment of the address-switching by measuring the voltage level at a predetermined time, or by measuring the time necessary for this rising voltage to reach a predetermined threshold level, said delay corresponding to the degradation of the cell by leakage. As a variant, while the readout circuit is disabled, the addressing signals are switched from selecting a written-in cell to selecting an unwritten-in cell to be tested, then the readout circuit is enabled, and the delay of the rising voltage is detected as above, but the time is measured from the moment at which the "enable" signal() is applied. The delays can also be detected at the output terminal ( $O_{\text{sub}o}$ ) of the readout circuit.

IPC 1-7

**G11C 29/00**

IPC 8 full level

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CPC (source: EP KR US)

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**EP 0214914 A2 19870318**; **EP 0214914 A3 19890503**; **EP 0214914 B1 19911204**; DE 3682732 D1 19920116; JP H0413800 B2 19920310; JP S6258500 A 19870314; KR 870003509 A 19870417; KR 900006143 B1 19900824; US 4862459 A 19890829

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