

Title (en)

REMOVABLE SIDEWALL SPACES FOR LIGHTLY DOPED DRAIN FORMATION USING ONE MASK LEVEL

Publication

EP 0216053 A3 19880120 (EN)

Application

EP 86109816 A 19860717

Priority

US 78053585 A 19850926

Abstract (en)

[origin: EP0216053A2] A method of using removable sidewall spacers (24) to minimize the need for mask levels in forming lightly doped drains (LDDs) (28,36) in the formation of CMOS integrated circuits. Aluminum or chemical vapor deposition (CVD) metals such as tungsten are suitable materials to form removable sidewall spacers (24) which exist around CMOS gates (18,20) during heavily doped source/drain region (20,28) implants. Other materials such as CVD polysilicon may also be useful for the sidewall spacers (24). The sidewall spacers (24) are removed before implantation of the lightly doped drain regions (28,36) around the gates (18,20). This implantation sequence is exactly the reverse of what is currently practiced for lightly doped drain (28,36) formation. The invention also includes the use of a differential oxide layer (32,34). A second set of disposable sidewall spacers (24) or the use of permanent sidewall spacers (40) form optional embodiments.

IPC 1-7

H01L 21/28; **H01L 21/82**; **H01L 29/08**

IPC 8 full level

H01L 21/033 (2006.01); **H01L 21/265** (2006.01); **H01L 21/336** (2006.01); **H01L 21/8238** (2006.01); **H01L 27/092** (2006.01); **H01L 29/08** (2006.01); **H01L 29/78** (2006.01)

CPC (source: EP US)

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Citation (search report)

- [A] DE 3324332 A1 19840112 - INTEL CORP [US]
- [X] PATENT ABSTRACTS OF JAPAN, vol. 9, no. 56 (E-302)[1779], 12th March 1985; & JP-A-59 197 161 (TOSHIBA K.K.) 08-11-1984
- [X] PATENT ABSTRACTS OF JAPAN, vol. 10, no. 1 (E-371)[2058], 7th January 1986; & JP-A-60 167 461 (HITACHI SEISAKUSHO K.K.) 30-08-1985
- [A] INTERNATIONAL ELECTRON DEVICES MEETING, San Francisco, CA, 13th-15th December 1982, pages 698-701, IEEE; A.C. HUI et al.: "An oxide masked P+ source/drain implant for VLSI CMOS"
- [A] PATENT ABSTRACTS OF JAPAN, vol. 9, no. 185 (E-332)[1908], 31st July 1985; & JP-A-60 055 658 (TOSHIBA K.K.) 30-03-1985

Cited by

US6153455A; US4868137A; EP1014441A1; DE3734304A1; DE3734304C2; EP0590652A3; EP0405293A1; US5399513A; EP0403368A1; FR2648622A1; EP0356202A3; US5087582A; US6551870B1; US6350652B1; US6274411B1; US6340828B1; US6573130B1

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