Title (en)

A DYNAMIC RANDOM ACCESS MEMORY DEVICE HAVING A SINGLE-CRYSTAL TRANSISTOR ON A TRENCH CAPACITOR STRUCTURE AND A FABRICATION METHOD THEREFOR

Publication

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Application

EP 86111645 A 19860822

Priority

US 78967585 A 19851021

Abstract (en)

[origin: US4649625A] Dynamic random access memory (DRAM) devices are taught wherein individual cells, including an access transistor and a storage capacitor are formed on a single-crystal semiconductor chip, and more particularly a three-dimensional dynamic random access memory (DRAM) device structure is described having a single-crystal access transistor stacked on top of a trench capacitor and a fabrication method therefor wherein crystallization seeds are provided by the single-crystal semiconductor area surrounding the cell and/or from the vertical sidewalls of the trench and wherein the access transistor is isolated by insulator. In the structure, a trench is located in a p+ type substrate containing heavily doped N+ polysilicon. A composite film of SiO2/Si3N4/SiO2 is provided for the capacitor storage insulator. A thin layer of SiO2 is disposed over the polysilicon. A lightly doped p-type epi silicon layer is located over the substrate and SiO2 layer. The access transistor for the memory cell is located on top of the trench capacitor. An N+ doped material connects the source region of the transistor to the polysilicon inside the trench. A medium doped p-region on top of the trench surface may be provided in case there is any significant amount of leakage current along the trench surface.

IPC 1-7

H01L 27/10; H01L 21/82

IPC 8 full level

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CPC (source: EP KR US)

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Citation (search report)

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Designated contracting state (EPC)

CH DE FR GB IT LI NL SE

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