

Title (en)
A DYNAMIC RANDOM ACCESS MEMORY DEVICE HAVING A SINGLE-CRYSTAL TRANSISTOR ON A TRENCH CAPACITOR STRUCTURE AND A FABRICATION METHOD THEREFOR

Publication
EP 0220410 A3 19890510 (EN)

Application
EP 86111645 A 19860822

Priority
US 78967585 A 19851021

Abstract (en)
[origin: US4649625A] Dynamic random access memory (DRAM) devices are taught wherein individual cells, including an access transistor and a storage capacitor are formed on a single-crystal semiconductor chip, and more particularly a three-dimensional dynamic random access memory (DRAM) device structure is described having a single-crystal access transistor stacked on top of a trench capacitor and a fabrication method therefor wherein crystallization seeds are provided by the single-crystal semiconductor area surrounding the cell and/or from the vertical sidewalls of the trench and wherein the access transistor is isolated by insulator. In the structure, a trench is located in a p+ type substrate containing heavily doped N+ polysilicon. A composite film of SiO₂/Si₃N₄/SiO₂ is provided for the capacitor storage insulator. A thin layer of SiO₂ is disposed over the polysilicon. A lightly doped p-type epi silicon layer is located over the substrate and SiO₂ layer. The access transistor for the memory cell is located on top of the trench capacitor. An N+ doped material connects the source region of the transistor to the polysilicon inside the trench. A medium doped p-region on top of the trench surface may be provided in case there is any significant amount of leakage current along the trench surface.

IPC 1-7
H01L 27/10; **H01L 21/82**

IPC 8 full level
H01L 27/10 (2006.01); **G11C 11/34** (2006.01); **H01L 21/74** (2006.01); **H01L 21/822** (2006.01); **H01L 27/00** (2006.01); **H10B 12/00** (2023.01)

CPC (source: EP KR US)
H01L 21/743 (2013.01 - EP US); **H01L 21/8221** (2013.01 - EP US); **H10B 12/01** (2023.02 - KR); **H10B 12/038** (2023.02 - EP US); **H10B 12/30** (2023.02 - KR); **H10B 12/373** (2023.02 - EP US)

Citation (search report)
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• [AP] EP 0167764 A2 19860115 - IBM [US]
• [A] SOLID STATE TECHNOLOGY, vol. 27, no. 9, September 1984, pages 239-243, Port Washington, New York, US; L. JASTRZEBSKI: "Silicon CVD for SOI: principles and possible applications"

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Designated contracting state (EPC)
CH DE FR GB IT LI NL SE

DOCDB simple family (publication)
US 4649625 A 19870317; AU 575499 B2 19880728; AU 6307186 A 19870430; BR 8604546 A 19870526; CA 1232362 A 19880202; CN 1005883 B 19891122; CN 86105868 A 19870610; DE 3688231 D1 19930513; DE 3688231 T2 19931104; EP 0220410 A2 19870506; EP 0220410 A3 19890510; EP 0220410 B1 19930407; ES 2003376 A6 19881101; HK 90993 A 19930910; IN 167820 B 19901222; JP H06101546 B2 19941212; JP S6298766 A 19870508; KR 870004513 A 19870511; KR 900002885 B1 19900501; ZA 866625 B 19870624

DOCDB simple family (application)
US 78967585 A 19851021; AU 6307186 A 19860923; BR 8604546 A 19860923; CA 518033 A 19860911; CN 86105868 A 19860909; DE 3688231 T 19860822; EP 86111645 A 19860822; ES 8602599 A 19861015; HK 90993 A 19930902; IN 596MA1986 A 19860728; JP 19301086 A 19860820; KR 860007237 A 19860830; ZA 866625 A 19860901