Title (en)

CMOS TECHNIQUE MULTISTAGE CARRY RIPPLE ADDER WITH TWO TYPES OF ADDER CELLS

Publication

EP 0224656 A3 19890524 (DE)

Application

EP 86111732 A 19860825

Priority

DE 3534863 A 19850930

Abstract (en)

[origin: EP0224656A2] A multi-digit carry ripple adder in CMOS technology and having two types of adder cells, in which an inverted carry input signal (Cin) is in each case applied to the adder cells of a first type (I) and a non- inverted carry input signal (Cin) is in each case applied to the adder cells of a second type (II) and in which a non-inverted carry output signal (Cout) is in each case output by the adder cells of the first type and an inverted carry output signal (Cout) is in each case output by the adder cells of the second type. The gate arrangements in each case required are formed in such a manner that the charging of the capacitance of the carry output occurs either via only one transfer transistor 117' or 118' acting as transfer gate or via the series circuit of only two transistors, one of which is in each case contained in gates III, II2 (or 13,14) and the second is in each case formed by a transfer gate 117 or 118. Due to the different carry paths, both the binary value "0" and the binary value "1" can be transferred without additional off-state losses. The transfer transistors (7,7',8,8') are not a component of a combination gate within the gate arrangement so that they can be designed to be of lower impedance than the remaining gate transistors. <IMAGE>

IPC 1-7

G06F 7/50

IPC 8 full level

G06F 7/501 (2006.01); **G06F 7/50** (2006.01); **G06F 7/506** (2006.01)

CPC (source: EP US)

G06F 7/501 (2013.01 - EP US); G06F 2207/3872 (2013.01 - EP US); G06F 2207/3876 (2013.01 - EP US)

Citation (search report)

- [A] EP 0155019 A1 19850918 - PHILIPS NV [NL]
- [A] EP 0143456 A2 19850605 - TOSHIBA KK [JP]
- [A] IBM TECHNICAL DISCLOSURE BULLETIN, Band 25, Nr. 4, September 1982, Seiten 1818-1819, New York, US; R.A. BECHADE et al.: "Inverted carry propagation chain"
- [A] SIEMENS FORSCH.- UND ENTWICKL.- BER., Band 5, Nr. 6, Dezember 1976, Seiten 324-326, Springer-Verlag, Berlin, DE; D. EICHRODT: "Rewarding application of transmission gates in MOS-LSI circuits"

Designated contracting state (EPC)

AT DE FR GB IT NL

DOCDB simple family (publication)

EP 0224656 A2 19870610; **EP 0224656 A3 19890524**; **EP 0224656 B1 19921230**; AT E84155 T1 19930115; DE 3687408 D1 19930211; JP H07117893 B2 19951218; JP S62113235 A 19870525; US 4931981 A 19900605

DOCDB simple family (application)

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