Title (en)

CIRCUIT FOR SERIAL DATA TRANSMISSION

Publication

EP 0229948 B1 19930317 (DE)

Application

EP 86116724 A 19861202

Priority

DE 3545293 A 19851220

Abstract (en)

[origin: EP0229948A2] The circuit arrangement comprises a transmitting device with several bit-parallel input information items, a serial data transmission link and a receiving device via which the transmitted data are appropriately converted into bit-parallel output information items for activating control elements or logic circuits, in which arrangement the data to be transmitted on the data transmission link form a data word which is composed of a start pulse, several information elements corresponding to the number of bit-parallel input information items which form one data block, and a defined data pause. By cascading several similar transmitting and receiving devices, the number of bit-parallel input and output information items can be changed, as a result of which the data word on the data transmission link is also changed by sequential adding-together of a corresponding number of data blocks having in each case the same number of information elements. <IMAGE>

IPC 1-7

B60R 16/02; G08C 15/12; G08C 25/00

IPC 8 full level

H04L 25/02 (2006.01); **B60R 16/02** (2006.01); **G08C 15/12** (2006.01); **G08C 25/00** (2006.01); **H04L 25/40** (2006.01)

CPC (source: EP US)

G08C 15/12 (2013.01 - EP US); **G08C 25/00** (2013.01 - EP US)

Cited by

FR2647998A1

Designated contracting state (EPC)

DE FR GB IT SE

DOCDB simple family (publication)

EP 0229948 A2 19870729; **EP 0229948 A3 19890426**; **EP 0229948 B1 19930317**; DE 3545293 A1 19870702; DE 3545293 C2 19890105; DE 3688060 D1 19930422; JP H0771087 B2 19950731; JP S62159548 A 19870715; US 5067076 A 19911119

DOCDB simple family (application)

EP 86116724 A 19861202; DE 3545293 A 19851220; DE 3688060 T 19861202; JP 30189886 A 19861219; US 68517991 A 19910415