

Title (en)

Three-dimensional integrated circuit and manufacturing method therefor.

Title (de)

Dreidimensionale integrierte Schaltung und deren Herstellungsverfahren.

Title (fr)

Circuit intégré tridimensionnel et son procédé de fabrication.

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Application

EP 87104091 A 19870320

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Abstract (en)

The invention relates to a three-dimensional IC stacked on a base plate comprising a unit semiconductor IC, A, which has each constituent IC (2a, 2b) either on a surface or on both surfaces of a substrate (1). The unit semiconductor IC has a plurality of conducting posts (4), buried in and penetrating through the substrate (1) and insulated therefrom, and also interconnection terminals (6, 7) on both sides of the substrate for connecting another unit semiconductor IC or the base plate. By stacking plural unit ICs on the base plate, a very large-scale IC can be fabricated. each constituent IC is formed on a bulk silicon substrate, so that excellent quality can be obtained. The invention can also be used for the fabrication of ROM structure such as a PROM or MASK ROM, using a single unit semiconductor IC, wherein a wiring for the ROM can be formed on a bottom surface of the substrate.

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C-Set (source: EP US)

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Cited by

US5846879A; EP1906441A1; US5426072A; EP0986104A4; FR2669468A1; EP0531723A1; FR2645681A1; EP2195843A4; US5902118A; DE4400985C1; US5741733A; US5767001A; KR100785821B1; EP0975472A4; CN115380372A; EP0374971A3; US5191405A; EP0577754A4; EP1503406A3; US5930596A; EP0610709A1; US5419806A; EP2024997A4; US6882030B2; US6388320B2; US6420209B1; US8329573B2; US6717254B2; US7998854B2; WO2009136873A3; WO9526568A1; WO2021150346A1; WO9845130A1; US11538762B2; WO0041241A1; WO9417553A1; WO0041240A1; WO9425981A1; WO9425982A1; WO2022026238A1; WO0041242A1; WO9601497A1

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