Title (en)

Variable delay circuit.

Title (de)

Schaltung mit veränderlicher Verzögerung.

Title (fr)

Circuit de retard variable.

Publication

EP 0244991 A2 19871111 (EN)

Application

EP 87303608 A 19870424

Priority

GB 8610888 A 19860503

Abstract (en)

A data processing system is described comprising a display terminal (10) and a processing unit (11). The display terminal includes a video timing generator (14) producing synchronisation signals (VSYNC, HSYNC). This triggers requests (QUAL) for the processing unit to supply video data. The display terminal includes a variable delay circuit (24) which measures the time delay between the outgoing request and the incoming data, and causes the synchronisation signals to be delayed by a corresponding amount. This ensures that the synchronisation signals are maintained in the correct timing relationship with the video data, irrespective of any unknown delays between the display terminal and the processing unit.

IPC 1-7

G09G 1/00

IPC 8 full level

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DOCDB simple family (publication)

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